

# **Toward a Plug-and-Play Approach for Active Power Factor Correction**

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Power electronics is following the trend of system integration in which a large part of the circuit is included in a microelectronics chip or module. Modularity is achieved by aggregating practically all the electronic in an IC or hybrid unit that may also include the power switch. This unit plus a line rectifier, inductor and bus capacitor are all that it takes to form an APFC system. It is demonstrated that dynamic stability is assured by this inherently robust control method. This plug and play solution will greatly simplify and reduce the cost of the design and manufacturing of APFC front ends.

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## **Introduction**

In recent years, power electronics technology is following the trend of system integration in which a large part of the circuit is included in a microelectronics chip or module. Modern integrated units (such as the TopSwitch of Power Integration Inc.) include not only the controller circuitry but also the drivers and power switches. Such "Smart Power" devices significantly reduce the effort associated with designing and compensating control loops, placement of the external devices on the PCB, eliminating some of the 'ground loops' problems etc. Ideally, one would like to have all the electronics in one unit such that, by adding few power passive elements, one will be able to construct a complete converter system in a "plug and play" manner. That is, without the need for special power electronics expertise. It would be advantageous, in particular, if the "plug and play" solution will relieve the user from the need to redesign the control loop for, say, different power levels. Clearly, this goal cannot be achieved by simply packaging conventional converter circuitry into a module or an IC chip. New control techniques and possibly new converter technologies will have to be developed before the "plug and play" solutions in power electronics can be realized. The feasibility of producing a modular Active Power Factor Correction (APFC) system was studied analytically and experimentally. The first step is already commercially implemented as a family of PFC IC – GPTC110XX. It is shown that the novel control scheme that does not need the sensing of the input voltage is highly compatible with the modular, plug-and-play concept. It is demonstrated that dynamic stability is assured by this inherently robust control method. This plug and play solution will greatly simplify and reduce the cost of the design and manufacturing of APFC front ends.

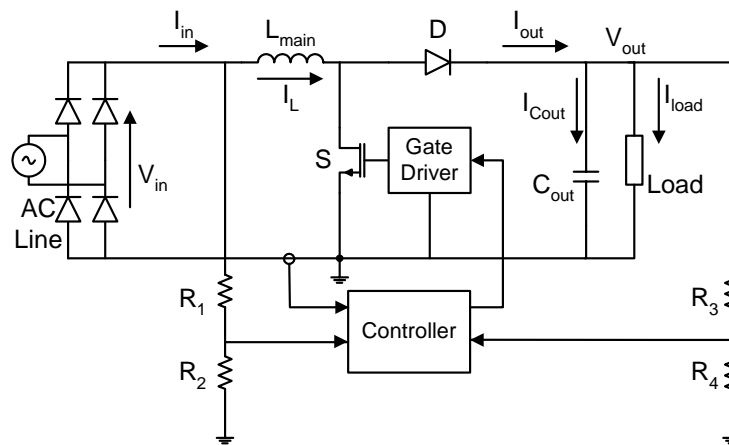


Fig. 1. Conventional CCM APFC approach.

A major drawback of the conventional implementation of the CCM APFC is the need for sensing the input voltage, namely the line voltage after rectification. Due to the switching effects, the input voltage is normally noisy and is susceptible to interference pick-up that may distort the reference signal and hence the input current. Also, the extra pin required for input voltage sensing will increase the number of pins of a modular device built in the conventional APFC scheme. Furthermore as experience engineers learned the hard way, designing an APFC system around a conventional controller is no easy task. As the practicing engineers know too well, making the inner (current) loop stable is tricky and fighting the ground loops is exhausting.

In this study we explored the possibility of utilising the APFC control method to realise a modular design for a CCM power stage in which all the electronics is packaged together in an IC or module (Fig. 2).

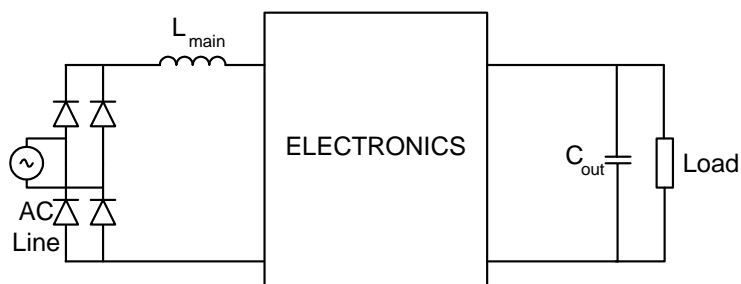


Fig. 2. Modular APFC approach.

### The Control Concept.

The analysis of the control concept has been published earlier<sup>5-7</sup>. We repeat here, for the sake of brevity, only the essentials. The novel APFC method is based on the Boost topology operating in the CCM. The system (Fig. 3) includes a power stage and a control scheme that senses the input current and produces a  $D_{off}$  duty cycle proportional to the average value of this current. The outer loop is used to trim the proportionality constant (between the input current and  $D_{off}$ ) to accommodate any given load. The principle of operation can be understood by considering an average model of Fig. 3 that represents the power stage (Fig. 4b).

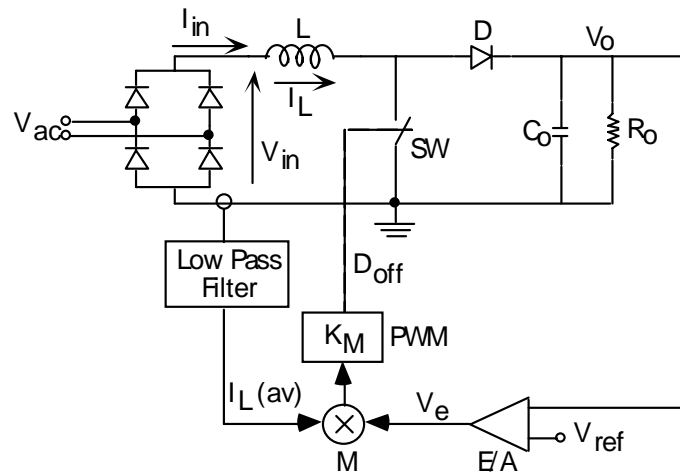


Fig. 3. Implementation of an APFC control scheme with no sensing of input voltage.

### The plug-and-play approach

The main obstacle in using the conventional CCM APFC control scheme of Fig. 1 for the modular plug-and-play approach is the large number of pins required for proper operation of the controller. Indeed, in addition to output voltage and input current sensing terminals one has to allow external connections for input voltage sense and compensation network of a current control loop.

In the novel control scheme, however, no sensing of the input voltage is required. This eliminates the interferences due to the noise that is typically found in conventional APFC approaches and reduces the number of external pins in the controller.

Moreover, the current control loop of the novel control method is unconditionally stable with tracking bandwidth of:

$$\frac{R_c}{2\pi L} = (BW_{in}) \quad (1)$$

As can be realised from inspection of the  $R_c/L$  term, this current control loop has a natural scaling capability. That is, in practice one would choose  $L$  to be proportional to  $R_c$  (the equivalent input resistance that defines the power level) and hence the loop gain will be the same for APFC stages designed for different power levels. This implies that there is no need to trim the phase compensation of the inner loop for each power level design. Consequently, the compensation network can be utilised inside the controller since no connection terminals for external compensation network are required anymore.

It should be pointed out that the novel control law:

$$V_{in}(av) = D_{off} V_o(av) \quad (2)$$

provides also an inherent current limiting capability stemming from the fact that a high input current will automatically increase  $D_{off}$ .

Based on these advantages the design of a universal controller that will fit any power level with minimum external pins is possible as shown on Fig. 4a. An APFC system built around such a controller is sketched on Fig. 4b. The time constant of a compensation capacitor  $C_{comp}$ , plus associated voltage divider, should be chosen so as to filter out a low frequency ripple, coming from the output of the converter's - as normally required in every APFC stage.

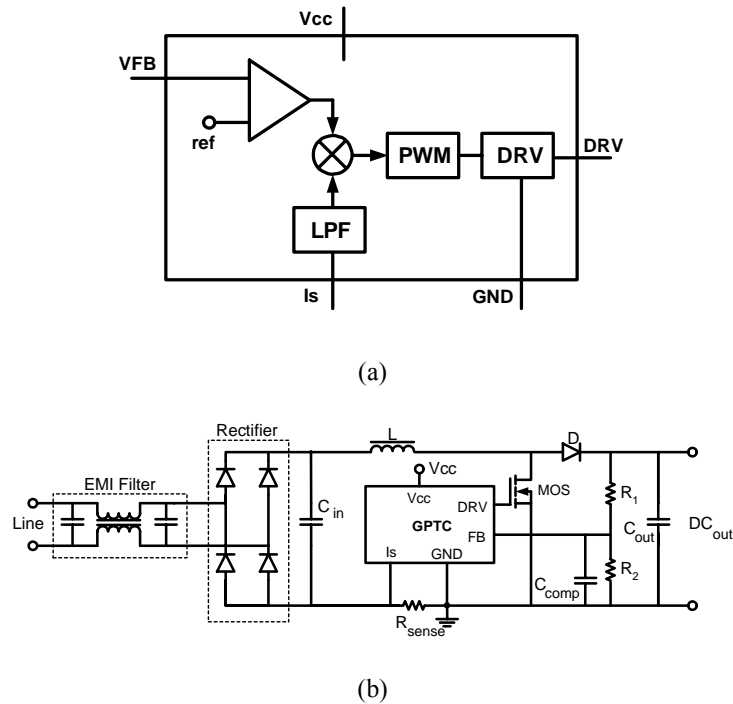


Fig. 4. Implementation of novel control scheme in a “discrete” form.  
A controller (a) and APFC stage built around it (b).

Combining the new controller together with a power switch in one package will result in a Self Containing Unit (SCU) (Fig. 10a). Since SCU requires only few external pins it can be packaged in a very standard 5 pins TO-220 or TO-247 package providing a low cost solution while integrated in APFC system (Fig. 5b).

### Experimental

To explore the concept developed above, one could use the GPTC110X EVB, an evaluation board for both GPTC1102A an 8 pin controller or the GPTC1101B a 14 pins controller that provide some extra features to the user. The tracking quality obtained experimentally is demonstrated by comparing the line current to the rectified input voltage (Fig. 6a). The measured harmonics were low, easily complying with the EN61000-3-2 standard (Fig.6b).

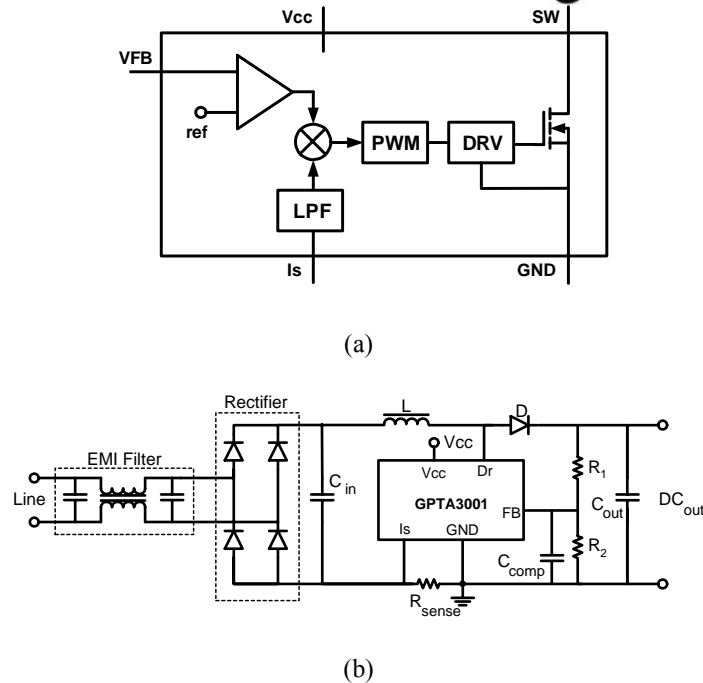
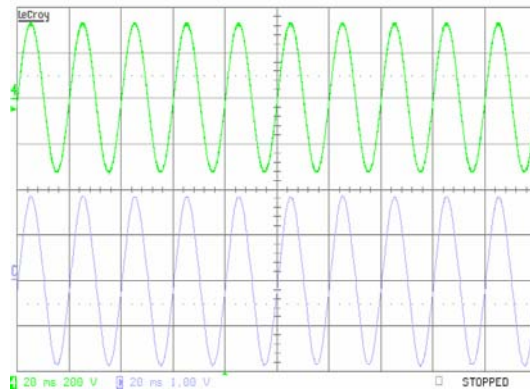


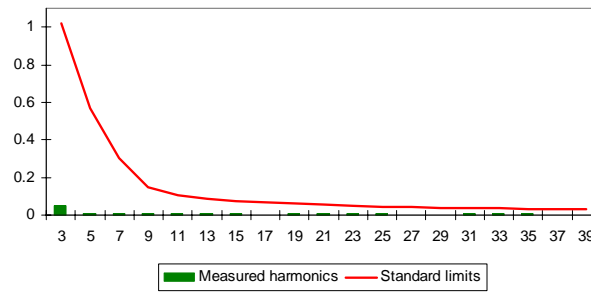
Fig. 5. Implementation of new control scheme in an IC form.  
Self-Contained Unit (a) and APFC stage built around it (b).

## Conclusions

The present study demonstrates that the “Smart Power” approach to APFC construction is feasible and it can lead to great simplification of APFC system design and integration - to a “plug and play” level. The analysis presented here shows that the advanced control law ensures adequate dynamic response and stability for any power level. For low power systems (up to about 250W), the approach led to an APFC IC family (GPTC101XX controllers and PF Switch-Assembly series) that will greatly simplify and reduce the cost of the APFC stage. All that would be required is to add the passive power components: rectifier, small high frequency by pass capacitor, inductor, and bus capacitor. A concept of possible implementation is shown in Fig. 7 (a) (b). An extra benefit of the smart power approach is the flexibility in the physical placement of the components in the system. For example, this is a result of the fact that the modular unit needs only two connections ports to function. Consequently, the One can thus conceive a line of devices that will cover the full power range of one-phase applications.

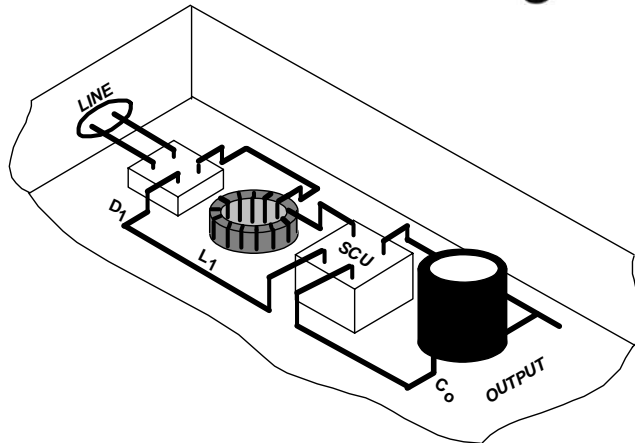


(a)

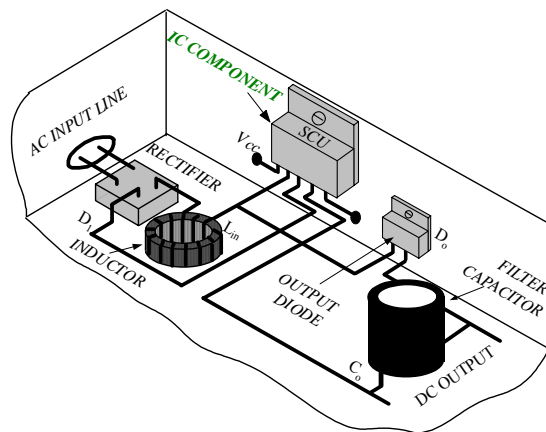


(b)

Fig. 6. Experimental results. (a) Upper trace: line voltage ( $230V_{rms}$ ). Lower trace: input current (1A/div). Horizontal scale: 20mS/div and (b) Compliance with EN61000-3-2 standard at the 300W level. Line: standard limits. Bars: measured harmonics.



(a)



(b)

Fig. 7. Modular implementation of advanced APFC technology. (a) Hybrid. (b) IC, monolithic or multichip.

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