

GPTC110XX

Continuous Current Mode

Power Factor Correction Controllers Family

Data Sheet

Application Note

**GPTC110XX Power Factor Correction Controllers Family**

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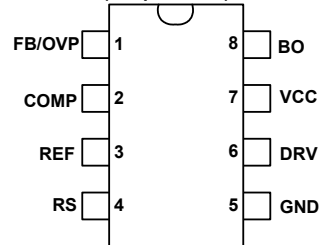
**GPTC110XX Power Factor Correction Controller Family**

**Features**

- Minimum external components count
- No sensing of the input voltage required
- Meets EN61000-3-2 Standard and IEC1000-3-2 recommendation
- High Efficiency
- Universal line operation
- Continuous-Conduction Mode operation
- Average-current mode PWM control
- Fixed frequency operation
- Unconditionally stable current control loop
- Cycle-by-cycle peak current limiter
- Start-up at full load
- Fast overvoltage protection
- Inherent average overcurrent protection
- Overtemperature protection
- Input voltage brown-out protection
- Internal/external soft start
- Improved noise immunity
- Standard package SOIC8

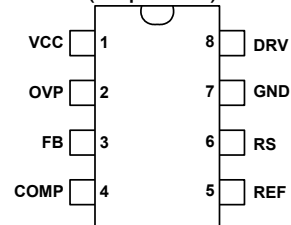
**GPTC1105X**

(Top view)



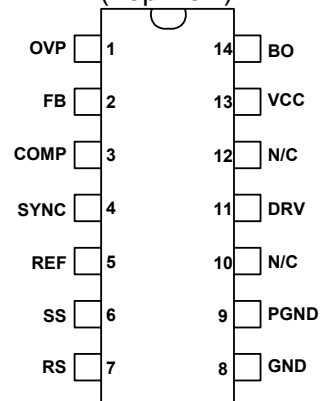
**GPTC1106X**

(Top view)



**GPTC1104X**

(Top view)



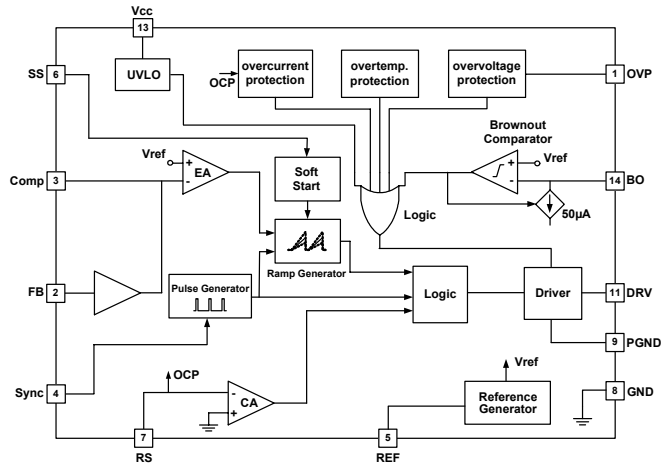
**DESCRIPTION**

The GPTC110XX series is designed to control APFC stages operating under Continuous-Conduction Mode (CCM) conditions. It provides near-unity power factor for universal input line voltage (85VAC-265VAC) with no need to sense the input voltage. The smart control algorithm guarantees stable and error-free operation over the whole operational range without compromising in THD. Leading edge control reduces the voltage ripple at the system's output. The GPTC110XX includes all the necessary housekeeping circuitry normally required in modern power systems. The design of a GPTC110XX based APFC stage is very simple and straightforward and requires minimum external components.

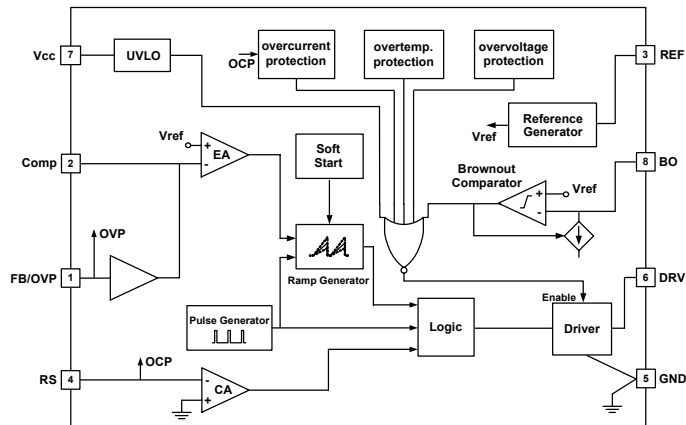
Available in the 8- and 14-pin SOIC and DIP packages.

BLOCK DIAGRAMS

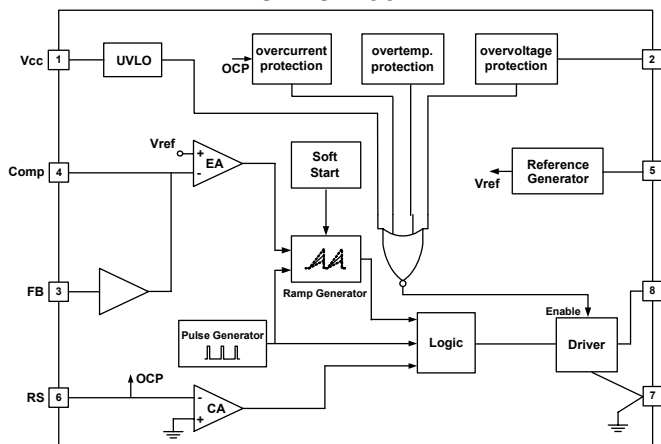
GPTC1104X



GPTC1105X



GPTC1106X



### ABSOLUTE MAXIMUM RATINGS

The maximum ratings may not be exceeded under any circumstances. All voltages are referenced to GND pin.

#	Symbol	Description	Min	Max	Unit
1	V <sub>CC</sub>	Auxiliary supply voltage	0	30	V
2	V <sub>PGND</sub>	Power ground voltage	-0.5	5	V
3	V <sub>BO</sub> , V <sub>SS</sub> , V <sub>SYNC</sub>	Input pin	0	V <sub>CC</sub>	V
4	V <sub>FB</sub> , V <sub>Comp</sub> , V <sub>REF</sub>	Input pin	0	10	V
5	V <sub>Rs</sub>	Input voltage current sense amplifier	-1	0	V
6	I <sub>DRV</sub>	Output Peak Current (2us)		±1500	mA
7	I <sub>BO</sub>	Brownout pin input current		50	µA
8	P <sub>tot</sub>	Power Dissipation T <sub>amb</sub> =85°C		TBD	mW
9	T <sub>jmax</sub>	Junction temperature		150	°C
10	T <sub>stg</sub>	Storage temperature range	-55	150	°C

### ELECTRICAL CHARACTERISTICS

Operational Range

#	Symbol	Description	Min	Typ	Max	Unit
1	V <sub>CC</sub>	Auxiliary supply voltage	8		30	V
2	T <sub>amb</sub>	Temperature range	-25		85	°C
3	D.C.	Duty cycle	0.01		1	sec/sec

DC Characteristics

DC characteristics contain the spread of values guaranteed within the specified supply voltage and temperature range and the technology process parameter range.

V<sub>CC</sub>=20V, CDRV = 10nF, T<sub>A</sub>=27°C for typical characteristics unless otherwise specified.

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Undervoltage lockout section</b>							
1	V <sub>CC_TON</sub>	VCC Turn-on threshold		10.45	11	11.55	V
2	V <sub>CC_TOFF</sub>	VCC Turn-off threshold		8.08	8.5	8.92	V

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply section</b>							
3	ICC	Operating Supply Current	fpulse = 100 kHz		17		mA
4	ICCl	Low Load Operating Current	fpulse=100kHz,		1.03	1.45	mA
5	I <sub>Q</sub>	Quiescent Current	VCC ≤ VCC <sub>TOFF</sub>		104	164	μA
6	I <sub>BO_H</sub>	BO input high current	V <sub>BO</sub> =5.5V		1		μA
7	I <sub>BO_L</sub>	BO input low current	V <sub>BO</sub> =4.5V	40	50	60	μA
8	V <sub>BO</sub>	BO threshold voltage		4.85	5	5.15	V
<b>Current loop amplifier section</b>							
9	V <sub>RS</sub>	Input voltage on RS pin		-0.8		0	V
10	VOS_CA	Input offset voltage			1	3	mV
11	G <sub>CA</sub>	Closed loop voltage gain			18.06		dB
12	BW	Closed loop bandwidth			6		kHz
<b>Voltage loop error amplifier section</b>							
13	G <sub>EA</sub>	Closed loop voltage gain			30		dB
14	BW	Closed loop bandwidth			37		kHz
15	VOH_EA	Output high voltage	Internal Rfb load ~3μA	6.2			V
16	VOL_EA	Output low voltage	Internal Rfb load ~12μA			20	mV
17	VOS_EA	Input offset voltage			2	6	mV
<b>Driver section</b>							
18	V <sub>GDRVH</sub>	DRV output voltage high	IDRV=-100mA	12.6	14.1	15.7	V
19	V <sub>GDRVL</sub>	DRV output voltage low	IDRV=100mA	0.18	0.27	0.53	V
20	I <sub>DRVpeak</sub>	Peak DRV current <sup>1)</sup>	VDRV=4V	750	1500	2500	mA
<b>Reference generator section</b>							
21	V <sub>REF</sub>	Reference voltage		4.9		5.1	V
22	dV <sub>REF</sub>	Initial accuracy of ref voltage	27°C	4.95		5.05	V

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Ramp generator section</b>							
23	CR <sub>CH</sub>	Max. to min. charge current			200		A/A
24	f <sub>PULSE</sub>	Pulse generator frequency	V <sub>CC</sub> = 8 to 30V, 27°C	90	100	110	kHz
<b>Synchronization section</b>							
25	V <sub>syncTH</sub>	Sync pin threshold voltage		2.05	2.1	2.2	V
26	f <sub>ext</sub>	External frequency range		90		110	kHz
<b>Overvoltage protection section</b>							
27	V <sub>OVPTh</sub>	Threshold voltage at OVP		5.4	5.5	5.6	V
28	V <sub>OVPHyst</sub>	Hysteresis voltage at OVP		0.75	0.8	0.85	V
<b>Overcurrent protection section</b>							
29	V <sub>RSOCPTh</sub>	OCP threshold voltage at RS		-0.66	- 0.69	-0.72	V
30	V <sub>RSOCPHys</sub>	OCP hysteresis voltage at RS		0.37	0.39	0.41	V
<b>Brownout section</b>							
31	V <sub>BOTh</sub>	Brownout threshold voltage		4.85	5	5.15	V
32	I <sub>BOhyst</sub>	Brownout hysteresis current		40	50	60	μA
<b>Overtemperature section</b>							
33	T <sub>JOT</sub>	Thermal shutdown junction temperature threshold		135	141	148	°C
34	T <sub>JHyst</sub>	Thermal shutdown hysteresis			14		°C
<b>Soft-start section</b>							
35	t <sub>del</sub>	Delay at turn-on	Pin open	17	21	27	msec
36	I <sub>del</sub>	Delay current for external capacitor	External capacitor	39	43	45	μA
37	V <sub>SSth</sub>	SS pin threshold voltage	External capacitor				

<sup>1)</sup> Without external gate resistor. Internally protected

### AC CHARACTERISTICS

AC characteristics contain the spread of values guaranteed within the specified supply voltage and temperature range and the technology process parameter range.

$V_{CC}=20V$ ,  $T_A=27^{\circ}C$  for typical characteristics unless otherwise specified.

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1	tr	Output Voltage Rise Time	CL=1nF VDRV 1 to 10V	10	20	30	ns
2	tr	Output Voltage Rise Time	CL=10nF VDRV 1 to 10V	45	100	150	ns
3	tf	Output Voltage Fall Time	CL=1nF VDRV 10 to 1V	10	20	30	ns
4	tf	Output Voltage Fall Time	CL=10nF VDRV 10 to 1V	45	100	150	ns

### ESD PROTECTION

All Pads of the IC are ESD protected (HBM 1kV).

### PIN DESCRIPTION

- VCC:**  
 Auxiliary supply input. Supplies power to all the internal circuits of the chip. Connect Vcc to a stable source of at least 17 mA above 11V. An external supply bulk capacitor is normally connected between this pin and signal ground (pin **GND**).
- FB:**  
 Feedback and error amplifier input. Used to sense output voltage through a voltage divider, which produces a nominal 5V.
- Comp:**  
 Compensation network input. The voltage loop compensation (usually a capacitor) is connected between this pin and signal ground (Kelvin connection to **GND** pin).
- BO:**  
 Brownout input. Used to detect line voltage failure. Disables PWM when below 5V. Connected to a voltage that is proportional to the average of the input rectified voltage. Provided with current hysteresis (internal current source of 50 $\mu$ A). Connect this pin to Vcc if not used.
- SS:**  
 Soft-start input. Internal soft-start circuitry provides 20mS delay at turn-on. Turn-on delay can be prolonged by connecting an external capacitor between this pin and the signal ground pin.

**GPTC110XX-SPD**

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- **GND:**  
Signal ground and reference point for all internal circuitry.
- **PGND:**  
Return terminal for high currents. Internally connected to the driver stage of the controller.
- **RS:**  
Current sense input. Internally connected to the negative terminal of current amplifier. External current sense resistor (Rsense) is connected between this pin and GND.
- **DRV:**  
Gate driver output. The output of the PWM is a MOSFET driver on DRV. This output is internally clamped to 15V so that the IC can be operated with Vcc as high as 30V.
- **OVP:**  
Overvoltage protection input. Senses the output voltage through an external divider. Provided with hysteresis. Disables the output driver if the output voltage is above the preprogrammed value.
- **REF:**  
Reference output. The output of an accurate 5V reference is provided to pin REF. An external 0.1 $\mu$ F or higher ceramic capacitor should be connected between this pin and the signal ground for best performance.
- **SYNC:**  
Synchronization input. A synchronization signal from the external source is connected to this input. Internally connected to GND via pull-down resistor. Leave open if synchronization is not required.

## APPLICATION INFORMATION

### Operating description

#### a. Basic equations

The basic configuration of an APFC stage built around the GPTC110XX is shown on Fig. 1. It is assumed that the boost stage is operated at constant frequency under CCM conditions.

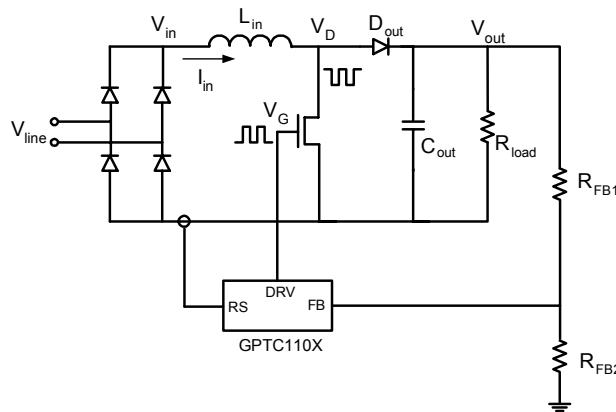


Fig. 1. GPTC110XX based APFC stage.

As shown on the timing diagram (Fig. 2) the instantaneous drain voltage ( $V_D$ ) is clamped to the output when the main switch is off and is zero when the switch is on. The low frequency component of the drain voltage can be thus found as:

$$\bar{V}_D = V_{out} D_{OFF} \quad (1)$$

where:

$\bar{V}_D$  is a low frequency component (average value over one switching period) of the drain voltage,

$D_{off} = 1 - D_{on}$ ,

$D_{on}$  is the duty cycle of the PWM signal that drives the main switch,

$V_{out}$  – output voltage of the power stage.

The control algorithm of GPTC110X generates  $D_{OFF}$  so as to be proportional to the average input current [1], i.e.

$$D_{OFF} = \left( \frac{R_e}{V_{out}} \right) \cdot \bar{I}_{in} \quad (2)$$

where:

$R_e$  is the equivalent input impedance of the power stage as "seen" by power line,

$\bar{I}_{in}$  is the low frequency component (average value over one switching period) of the input current.

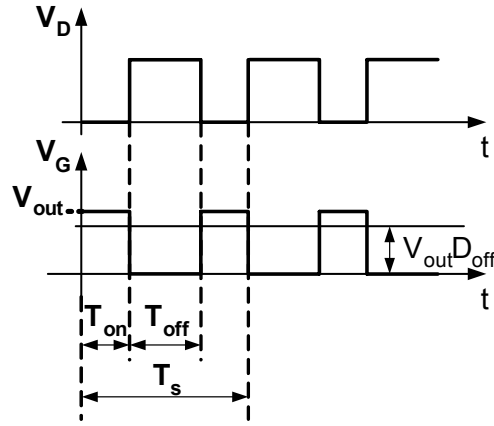


Fig. 2. Key waveforms.

Substituting (3) into (2) and neglecting the ripple at the output of the power stage yields:

$$\bar{V}_D = R_e \cdot \bar{I}_{in} \quad (3)$$

As one can see from (3), if  $D_{OFF}$  is modulated according to (2) the average input current follows the average drain voltage  $V_D$ .

Supposing a steady state, the average voltage on the input inductor must be zero. Otherwise the current will go to very high values. That is, the average voltages on both sides of the input inductor are equal, i.e.:

$$V_{in} = \bar{V}_D = R_e \cdot \bar{I}_{in} \quad (4)$$

or rearranging:

$$\frac{V_{in}}{\bar{I}_{in}} = R_e \quad (5)$$

This means that the average input current follows the input voltage, as required in power factor correction applications, emulating an equivalent input impedance of  $R_e$ .

b. Control algorithm implementation.

According to the control algorithm used in the GPTC110XX, the duty cycle,  $D_{off}$ , must be proportional to the average input current, while the proportionality coefficient is set according to the operating point which in turn is dictated by the line voltage and the load.

It is accomplished by utilizing two control loops (Fig. 3): a current control loop, responsible for input current shaping and a voltage control loop which adjusts the input current amplitude according to the power consumed by the load.

The current control loop senses the input current and filters it to reconstruct the average value. The resulting signal, which is proportional to the average input current, is provided to the PWM which in turn generates  $D_{off}$  which is proportional to the average input current as well.

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The voltage control loop adjusts the ratio between the input current and Doff to keep the output voltage at its nominal value for any operating point (i.e. line voltage and power level).

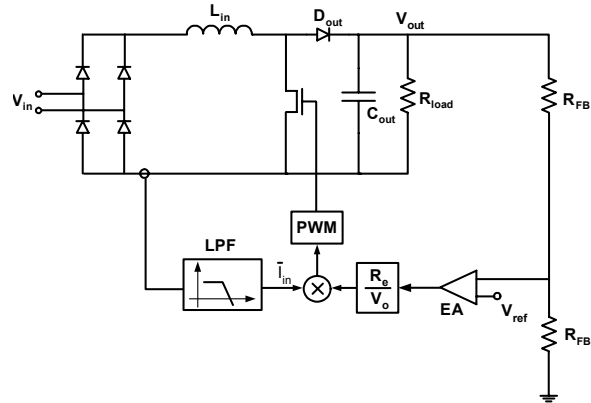


Fig. 3. Control algorithm implementation.

**Supply and Under-Voltage Lockout section.**

An internal Under-Voltage Lockout unit (UVLO) monitors the voltage at the Vcc pin and enables an internal output driver when it exceeds 11V. The driver is disabled if the external supply falls below 8.5V. The typical current consumption of the GPTC110XX in standby mode (Vcc<8.5V) is as low as 130µA. This low consumption requirement of GPTC110XX during start-up allows the use of a high-resistance bootstrap resistor in auxiliary power supply circuitry minimizing its power dissipation and power rating.

The typical current consumption of the IC while not driving (quiescent current) is 1.5mA. The total power consumption can be calculated as the sum of the quiescent current and the current required to drive the input capacitance of the external MOSFET, i.e.:

$$I_T = I_{qa} + C_{in} V_{GS} f_{sw} \tag{6}$$

where:

- $I_T$  – total current consumed by the IC,
- $I_{qa}$  – quiescent current,
- $C_{in}$  – MOSFET's input capacitance,
- $V_{GS}$  – MOSFET's gate-to-source voltage,
- $f_{sw}$  – switching frequency.

**Soft-start section.**

The GPTC110XX includes soft-start circuit which limits the duty cycle of the main switch at turn-on, preventing damage that might be caused to the APFC during the initial transients.

If no external capacitor is connected between the SS pin and the ground (pin SS is open), an internal timing circuit provides a soft-start delay of about 20mS. During this delay the slope of the ramp generator is raised from zero value to its nominal value determined by the operating point. As explained below (see PWM section) the duty cycle is generated in the GPTC110XX

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by comparison of a ramp signal and a threshold value set by the current amplifier output. The shallower the slope the later the ramp meets the threshold level (See Fig. 4) and the smaller the duty cycle is. As a result the duty cycle increases from zero (switch is off) to its nominal value, dictated by the input and output voltages (see Fig. 4).

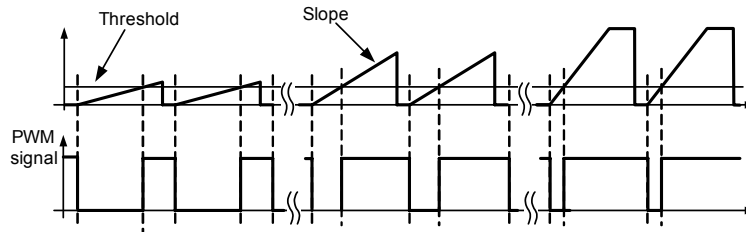


Fig. 4. Ramp and PWM signal during the start up.

The internal soft-start delay can be extended by connecting an external capacitor between the SS pin and the ground. The capacitor in this case is charged by an internal current source of  $40\mu\text{A}$ . The soft-start delay ends when the voltage at the SS pin reaches 5V.

When the external capacitor is connected the overall turn-on delay  $t_{\text{del}}$  is given by:

$$t_{\text{del}} = 20\text{ms} + \frac{C_{\text{ext}}}{40\mu\text{A}} 5\text{V} \quad (7)$$

The soft-start circuitry is reactivated in case of an overvoltage or the input line failure (if brown-out protection is used).

### Current loop section.

The current loop generates a signal which is proportional to the average inductor current. The latter is compared in the PWM block to the ramp signal generated by the ramp generator. An instantaneous input current can be sensed using a sense resistor or any other current-sensing technique. The resulting (negative) signal must be fed to the RS pin which is internally connected to the input of a narrow bandwidth inverting current amplifier (see Fig. 5). The signal on the RS pin is then inverted, amplified and filtered out to reconstruct the average value of the input current ( $V_{\text{CAout}}$ ). The current amplifier of the GPTC110XX is internally compensated and has a gain of 12. The bandwidth of the current amplifier is 6kHz (typical, see "Current loop amplifier section" in "DC characteristics") and is chosen so as to filter out the high frequency component of the input current. On the other hand this bandwidth is wide enough to pass all the significant harmonics of the rectified sinusoidal wave which are supposed to appear on the RS pin [2].

The current loop of the GPTC110XX is unconditionally stable and requires neither an external compensation network nor an external filter.

For the given power level and input voltage the bandwidth of the current loop depends on the input inductor as follows [2]:

$$\text{BW}_{\text{CL}} = \frac{V_{\text{rms}}^2 \eta}{2\pi L P_{\text{out}}} \quad (8)$$

where:

$BW_{CL}$  – current loop bandwidth,

$V_{rms}$  – RMS value of the input voltage,

$\eta$  - efficiency of the power stage,

$L$  – input inductor,

$P_{out}$  – output power.

It should be also noted that the actual bandwidth of the current loop is limited by the bandwidth of the current amplifier (6kHz typical).

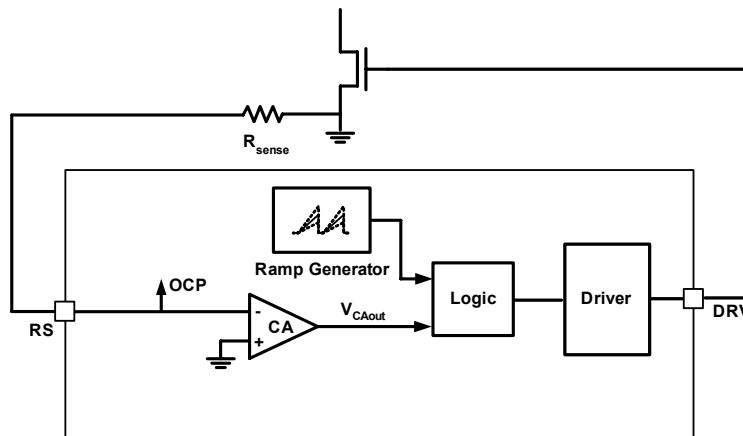


Fig. 5. Current control loop.

The maximum output voltage of the current amplifier is 6.49V typical. Assuming the gain of 8 the maximum absolute value at the RS pin should not exceed  $6.49V/8=0.81V$  in the steady state. If the maximum instantaneous input current is  $I_{in\_pk}$  the maximum value for the sense resistor can be obtained from eq. 9 as follows:

$$R_s \leq \frac{0.81V}{I_{in\_pk}} \quad (9)$$

In practice, the value of  $R_s$  will be usually dictated by power dissipation considerations.

If the voltage at pin RS falls below -0.69V (typical) the overcurrent protection is activated and the output driver disabled (see Overcurrent Protection section).

The voltage on pin RS must not exceed -0.8V under any circumstances.

#### Voltage Control Loop.

The voltage loop measures the output voltage and adjusts the slope of the ramp signal so as to keep the output voltage stable over the whole operational range.

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The output voltage is measured by the FB pin usually via an external resistive attenuating network. The voltage at pin FB is provided to the inverting input of a voltage error amplifier through the internal Non-Linear Amplifier (NLA). The noninverting input of the voltage error amplifier is tied to the output of the internal reference generator which produces typically 5V (Fig. 6).

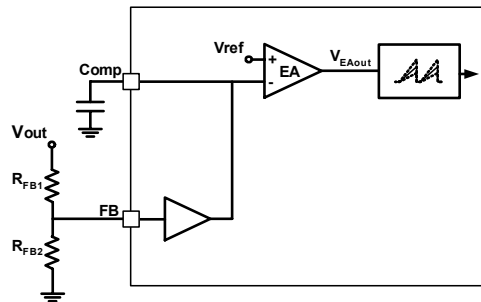


Fig. 6. Voltage control loop.

#### a. Voltage Error Amplifier (VEA).

The VEA is configured as a noninverting operational amplifier with a gain of 30dB and a bandwidth of 37kHz (typical, see Voltage loop error amplifier section in "DC characteristics").

The voltage control loop is compensated by an external compensation network which is connected between the pin Comp and the ground. The bandwidth of the voltage control loop will be determined as follows (see Fig. 6):

$$BW_{VL} = \frac{1}{2\pi C_c (R_{NLA} + R_{F1} \parallel R_{F2})} \quad (10)$$

where:

$BW_{VL}$  – bandwidth of voltage control loop,

$R_{NLA}$  – an equivalent resistance of NLA under steady state conditions.  $R_{NLA}$  typical is 100k $\Omega$ .

The bandwidth of the voltage control loop needs to be small enough to filter out the ripple at the output terminals which may otherwise penetrate the voltage loop, modulating the slope of the ramp and distorting the input current. Assuming the ripple frequency of 100-120Hz (twice the line frequency) the bandwidth of the voltage loop should not exceed 10-15Hz.

#### b. Fast dynamic response.

Since the bandwidth of the voltage control loop required in APFC applications is very small, the dynamic response of a typical APFC stage is obviously poor. As a result one can expect quite large over- or undershoots at the output of the APFC stage if the input line and/or output load is changed.

GPTC110XX is provided with a proprietary "smart" NLA which improves the transient response of the APFC stage substantially reducing the overshoot (or undershoot) at the output that would be observed otherwise.

Due to its "smart" behavior, NLA acts as a pure resistor under steady state conditions while charging/discharging the compensation capacitor very quickly during the transient caused by either load or input line changes.

PWM section.

The PWM section comprises of a pulse generator, a ramp generator, a PWM comparator and an RS-latch.

a. Ramp generator.

The duty cycle is generated by comparison of the sawtooth signal issued by the ramp generator with the voltage at the output of the current amplifier (Fig. 7).

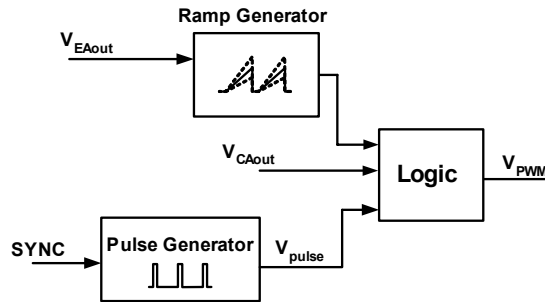


Fig. 7. PWM section.

As mentioned earlier (Current Loop Section), the signal seen at the current amplifier's output is proportional to the averaged input current.

That is, the duty cycle is the result of a comparison of the ramp signal with a signal that is proportional to the average input current. In this way the duty cycle ( $D_{off}$ ) is proportional to the average input current as required by the control law (2). Fig. 8 shows the duty cycle for different input currents. It is assumed that the input line voltage and the load are unchanged (constant slope).

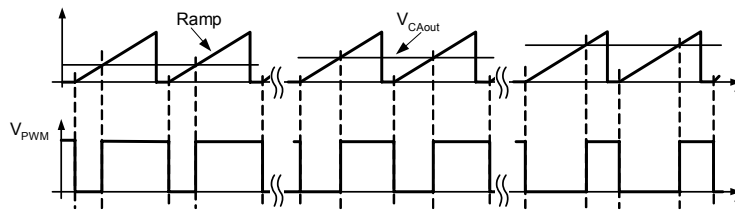


Fig. 8. Duty cycle at different input currents. The slope is constant.

As can be seen from Fig. 8 the higher the input current, the later the ramp signal meets the threshold and the higher the duty cycle ( $D_{off}$ ) is.

If the input voltage and/or the output load changes, the voltage control loop changes the slope so as to keep the output voltage unchanged. This is shown on Fig. 9 which indicates the duty cycles for various operating points at the same input current.

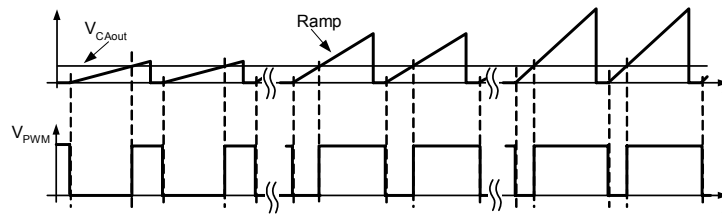


Fig. 9. Duty cycle at different operating points. The input current is unchanged.

If for example the output voltage tends to go up, the voltage control loop will decrease the slope. As seen in Fig. 9, this will reduce the duty cycle (increase  $D_{off}$ ) and thus the output voltage will go back to its nominal value.

b. Pulse generator.

The operating frequency of the GPTC110XX is set internally to 100kHz by an internal oscillator which generates positive pulses ( $V_{pulse}$ ) (Fig. 10).

As shown in Fig. 10 the positive-going edge of the pulse discharges the ramp signal to zero in every cycle. The next cycle is initiated by the negative edge of the pulse. Once this happens, the driver is set to its off state and the ramp starts rising with the slope determined by the VEA.

According to the control algorithm (2) the duty cycle ( $D_{off}$ ) must be able to take very low values if the input current is close to zero. Otherwise the input current will be distorted near the zero-crossing area.

As one can see from Fig. 10 the ramp signal starts rising at the beginning of the "off" time. Consequently  $D_{off}$  can be essentially zero, as required by (2).

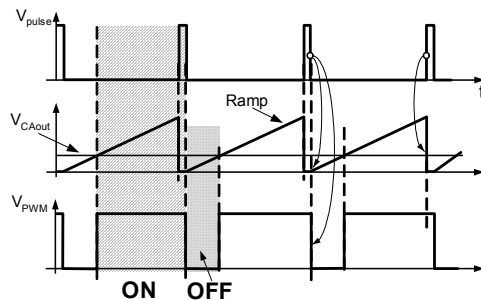


Fig. 10. Achieving zero "OFF" time.

If the threshold set by the current amplifier ( $V_{CAout}$ ) is higher than the peak value of the ramp (see Fig. 11) the ramp signal can not reach the threshold value. In this case the "on" time will be initiated by the positive-going edge of the oscillator pulse  $V_{pulse}$ . Consequently, the minimum "on" time is limited to the width of the oscillator pulse.

The width of the oscillator pulse is determined by the pin DClim (see below).

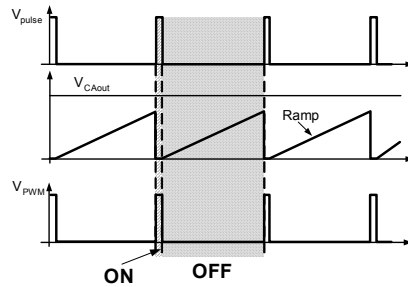


Fig. 11. Minimum "on" time.

c. Minimum "on" time.

The GPTC110XX is designed to support the snubber circuitry which helps to reduce the losses due to reverse recovery of the output diode. As will be explained below (Soft switching section) this circuitry requires a minimum "on" time for proper operation.

The minimum "on" time is programmed by pin DClim.

The DClim pin should be left open (unconnected) if a snubber is not used. In this case the minimum  $D_{on}$  will be about 1%.

By connecting the DClim pin to Vcc the minimum "on" time is set to about  $1.7\mu S$ . This is the minimum time required to reset the snubber circuitry.

d. Synchronization.

The GPTC110XX's oscillator can be synchronized with an external pulse source. A rectangular wave must be applied to pin SYNC if synchronization is required. The characteristics of the external source can be found in the "Synchronization section" of DC characteristics.

An external pulse source is masked (ignored) during the soft-start delay.

Pin SYNC is internally connected to ground via a pull down resistor. Leave this pin open (unconnected) if no synchronization is needed.

The GPTC110XX uses a leading edge modulation method and hence its synchronization with a subsequent DC-DC stage (which normally employs trailing edge modulation) will naturally reduce the high frequency ripple on the PFC's output capacitor without the need for additional circuitry.

Protection circuitry.

GPTC110XX contains several internal protection circuits to prevent the APFC stage from being damaged in the cases of very high output voltage, overload, overheating and input line failure.

All the protection circuits disable the output driver when activated (Fig. 12).

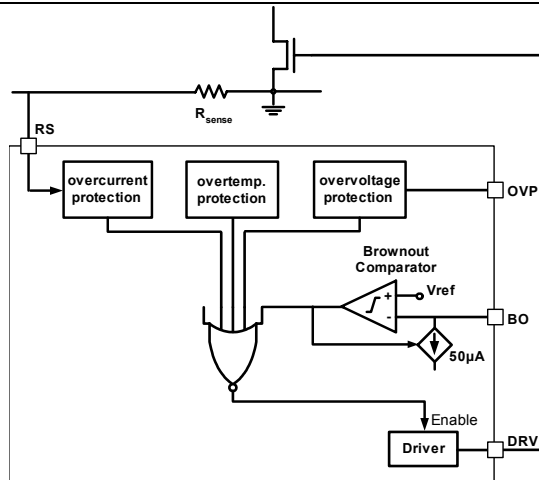


Fig. 12. Protection circuits and logic.

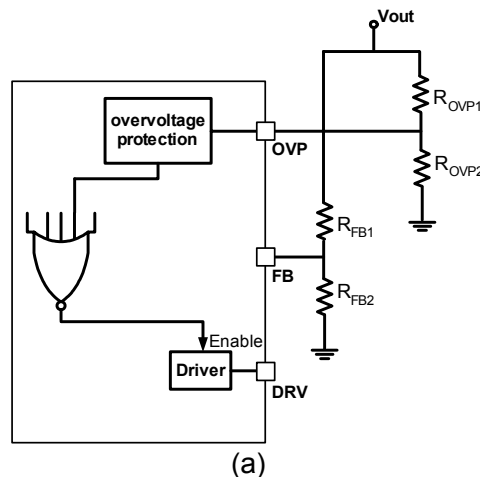
a. Overvoltage protection.

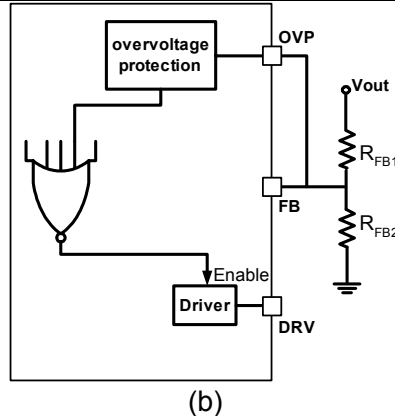
An internal overvoltage protection circuit senses the voltage on pin OVP. The OVP pin can be connected to the output voltage in one of two possible ways (Fig. 13):

1) Pin OVP is just connected to the FB pin (Fig. 13a) which senses the output voltage via an external voltage divider  $R_{FB1}$ ,  $R_{FB2}$ .

This arrangement can be used in a minimal configuration when the external element count and/or space saving considerations are of prime importance.

2) Pin OVP is connected to the output voltage terminals via an additional external voltage divider  $R_{OVP1}$ ,  $R_{OVP2}$  (Fig. 13b). That is, the overvoltage circuitry senses the output voltage independently of the voltage control loop. In this way the overvoltage conditions will be detected even if either  $R_{FB1}$  or  $R_{FB2}$  gets corrupted.





(b)  
Fig. 13. Measuring output voltage for OVP protection.  
(a) Using an additional voltage divider. (b) By connecting to the FB pin.

The overvoltage circuitry disables an internal output driver if the voltage at pin OVP is above 5.5V (typical). When this voltage falls below 4.7V the driver is enabled and the soft-start circuitry is activated.

b. Overcurrent protection.

The cycle-by-cycle overcurrent protection disables the output driver if the voltage at pin RS falls below -0.69V (typical).

The driver is released if the input current decreases such that the voltage at pin RS rises to -0.3V (typical). The overcurrent circuitry has a small inherent delay to prevent parasitic oscillations.

c. Brownout.

The brownout comparator is designed to detect failure of the input line. This feature is optional and can be deactivated by connecting pin BO to Vcc.

The brownout detection circuitry, if used, senses the voltage at pin BO. This pin is normally fed by an external low pass filter which averages the input voltage (Fig. 14).

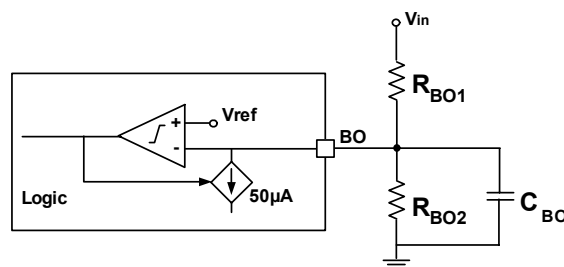


Fig. 14. Brownout detection.

The BO pin is connected internally to the inverting input of the brownout comparator. If the voltage at the BO pin falls below 5V the brownout comparator trips to its high state disabling the output driver and turning on a 50µA internal current hysteresis source (Fig. 14). The latter flows via  $R_{BO1}$  and  $R_{BO2}$ , decreasing the voltage at pin BO. The brownout comparator snaps back to

## GPTC110XX-SPD

its low state if the voltage at the BO pin rises above 5V. Once this happens the hysteresis current source turns off, the output driver is enabled and the soft start circuitry is activated.

The brownout detection circuitry of GPTC110XX allows the programming of both the input voltage failure threshold and the hysteresis value.

Assuming a rectified sinusoidal input voltage the brownout threshold value is given by the following equation:

$$V_{in_{th}}(rms) = \frac{\pi}{2\sqrt{2}} \cdot \frac{R_{BO1} + R_{BO2}}{R_{BO2}} \cdot 5V \quad (11)$$

where:

$V_{in_{th}}(rms)$  – the rms value of the input voltage at which the line failure will be detected

$R_{BO1}$ ,  $R_{BO2}$  – resistors in Fig. 14.

To release the brownout comparator the input voltage must be higher than  $V_{in_{th}}(rms)$  by the value given in (12) (hysteresis value):

$$V_{hys} = 50\mu A \cdot R_{BO1} \quad (12)$$

## Reference generator section.

The reference generator provides a stable reference of 5V for all the internal circuitry of the GPTC110XX. The overall accuracy of the ramp generator is trimmed to 2%. Its variation over the temperature range is only 1%.

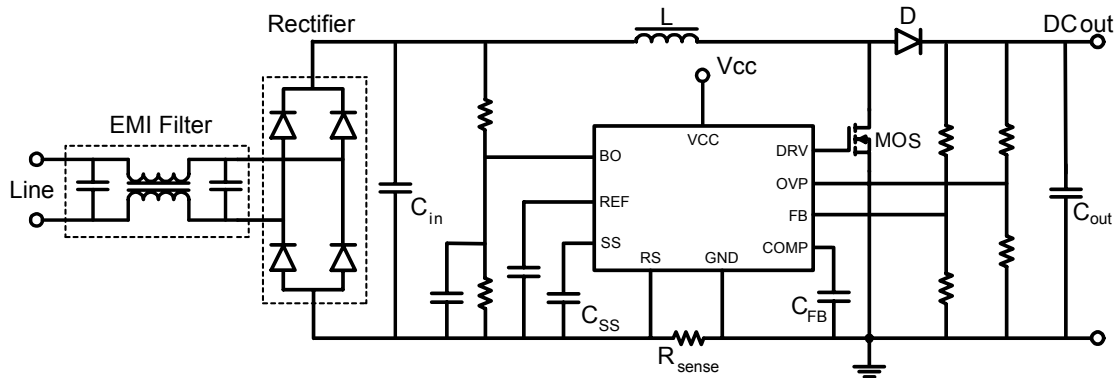
## Driver section.

The output of the GPTC110XX (DRV pin) is fed by a totem pole MOSFET driver. The DRV pin is internally clamped to about 15V, so the IC can be operated with  $V_{cc}$  as high as 30V without the risk of damage to the main MOSFET. The driver is capable driving a capacitive load directly – no external series resistor is required. Typical rise and fall times are 20nS with 1nF load. The maximum output current is 1.5A.

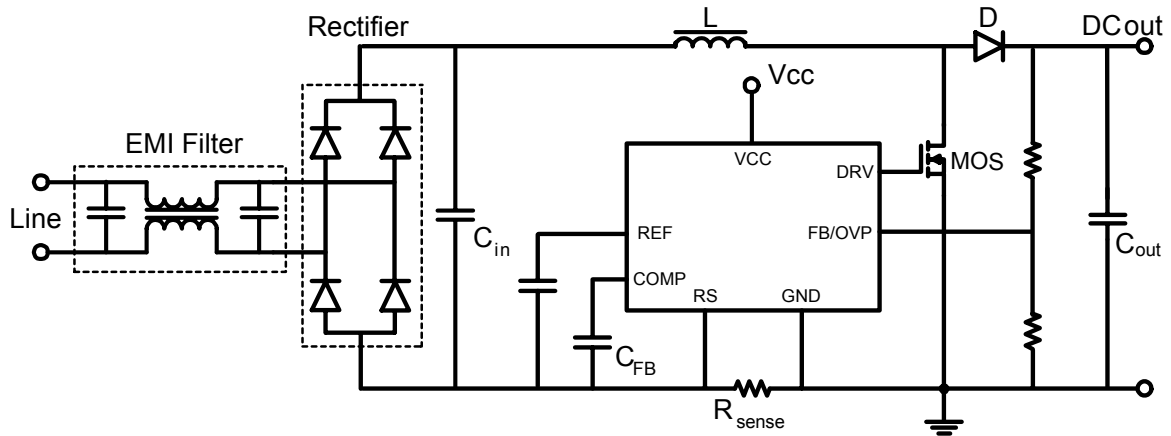
The driver is in its low state when  $V_{cc}$  is below 8V. It is disabled when one of the protection circuits is activated.

**TYPICAL APPLICATIONS**

Functional application of the PFC controller GPTC1104 using all functions



Functional application of the PFC controller GPTC1105 in minimal configuration





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**NOTES**